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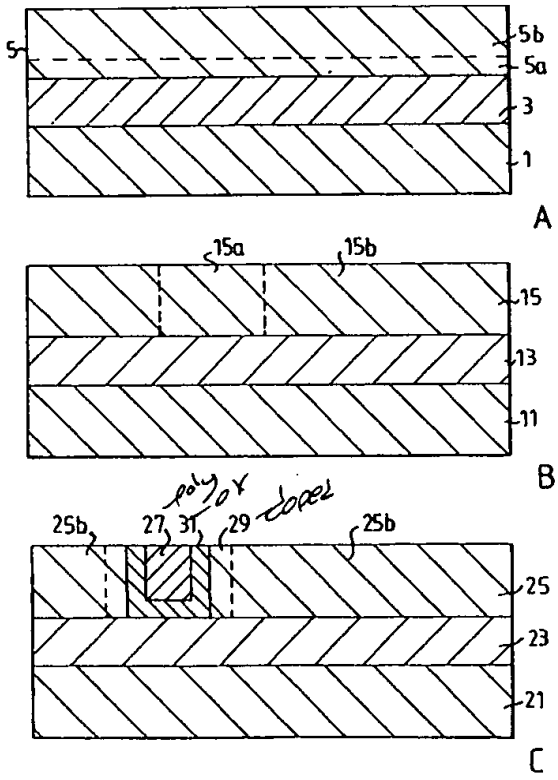
(57) Abstract

A semiconductor component is disclosed, having a device layer comprising at least one lateral insulating area, such as a trench, the walls of said lateral insulating area being covered with a gettering layer functioning as a getter when processing the semiconductor component. Preferably, the gettering layer is substantially without acceptor and/or donor type impurities, or the concentration of acceptor and/or donor type impurities is not greater than the concentration of acceptor and/or donor type impurities in the trench wall. The gettering layer comprises a gettering material such as polysilicon or porous silicon, or a silicide, and is covered with a layer of an insulating material. A method for the manufacturing of such a component is also disclosed.



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Semiconductor Component and Manufacturing Method for Semiconductor Components

Technical Field

The present invention relates to semiconductor components, and especially to the reduction of contamination in such components.

Background

A problem in the manufacturing of semiconductor components is that such components tend to be susceptible to contamination by impurities, especially metallic impurities. Several different techniques, some of which will be discussed in more detail in the following, are used to capture such impurities in regions of the component where they will do no harm. The regions used for this purpose are known as getter centres, and the process is known as gettering.

Metal such as Cu, Fe, Al, Cr, W, and others, if present on the silicon surface while the component is being processed, for example at a high temperature, may diffuse into the silicon crystal, causing the properties of the silicon components to deteriorate. For example, the leakage current in diodes will be increased. The above mentioned types of metallic impurities diffuse fast in silicon but may be captured in areas where the silicon crystal is not perfect, such as areas with many dislocations or other defects. This is referred to as gettering, and asubstance that tends to capture impurities is referred to as a getter. If gettering occurs in an uncontrolled way, for example for bipolar components it may lead to a short circuit between the emitter and the collector. For MOS components it may lead to a reduced oxide quality.

Of course the rinse, anneal and other process steps currently used are designed to minimize the risk of metal pollution on the surface, but the pollution can never be completely eliminated. Therefore, ways of further improving the immunity of the components to contamination are used. As most metallic impurities diffuse fast in

silicon but may be captured in areas with many defects, the back of the silicon wafer may be processed in such a way that impurities present in the wafer or introduced in the wafer during processing will be concentrated to the backside.

One technique of removing metallic impurities from the silicon regions in which the sensitive parts of the components are located involves intentionally damaging the back surface of the wafer. Mechanical abrasion methods such as lapping or sand blasting have been used for this purpose. Other techniques use a focused laser beam to create the damages at the back of the wafer. During the device processing, most of the metallic impurities will then diffuse to the damaged region.

Another technique is to deposit polycrystalline silicon (polysilicon) at the backside. The impurities will then diffuse to the grain boundaries inside the polysilicon layer. Usually, a polysilicon layer is used in combination with a high concentration of phosphorous in the polysilicon. The mechanical stress inside the heavily doped regions (caused by the high concentration of phosphorous) further improves the capability to getter impurities.

The concentration of metallic impurities in the part of the silicon comprising the components can then more easily be kept at a low level during processing.

Silicon on Insulator (SOI) materials are particularly well suited for use in semiconductor components for several reasons. They offer latchup immunity, galvanic isolation between components and reduced parasitic capacitance.

The most commonly used SOI material is a thin silicon layer, typically between 500Å and 30 μm thick, on an isolating layer, for example a silicon oxide. Because of the buried oxide the SOI components are particularly sensitive to contamination by metals and metal ions to which the silicon surface is exposed during the processing of the silicon.

In the case when the silicon layer comprising the components has been separated from the remaining part of the substrate by an isolating film, as is the case for SOI material, this isolator can, however, function as a diffusion barrier, preventing the contamination from moving to a portion of the substrate in which they can cause no harm. The above mentioned methods therefore are not effective for most types of SOI materials.

Alternative solutions have been presented to increase the immunity of SOI materials to metal contamination, in order to improve the yield when producing SOI components. The most commonly used method is to dope a part of the silicon device layer. This heavily doped part will then attract the impurities in the same way as the doped back of a standard silicon wafer. The heavily doped layer may later, for some component types, function as part of the collector.

In a similar way, a thin layer of polycrystalline silicon or porous silicon may be provided between the buried isolator and the component layer. A further alternative is to introduce damages and defects in the silicon area nearest to the buried isolator. This may be done, for example, by creating oxidation damages in the substrate. It is, however, hard to ensure that such damages will not proceed into a sensitive part of the component.

The above mentioned methods do not function well for component types where the whole silicon layer is part of the active area of the component, especially when the silicon layer is thin. The introduced doped area may also disturb the electrical field around the component.

Therefore, other alternatives have been presented utilizing lateral diffusion of metallic impurities to getter areas. This may be done, for example by introducing an additional masking step in the process, enabling the heavy doping of some areas of

the silicon wafer. It has been shown that lateral gettering may function up to a distance of 1 mm away from the heavily doped areas. Another alternative is to utilize the masking steps needed to laterally isolate the components from each other. For the lateral isolation, for example, trench technology may be used.

Japanese Patent Specification JP 727 31 21 discloses a method of using a trench wall as a getter centre by implanting impurity ions into the side walls of the trench. The component is then heat treated to effect the gettering, and the region of the trench wall comprising the impurities is removed. Rotary implantation of carbon, phosphorus or boron ions is used at predetermined angles. This solution requires the implantation to be made at a well defined angle, and the rotation of the wafer during implantation. These two restrictions limit the design possibilities in an undesirable way. For certain types of components, however, the trench wall cannot be too heavily doped, as this would disturb the electric field in these components and reduce their performance.

The method according to the invention will be particularly useful to gettering in SOI components. It is however applicable to any other kind of semiconductor component as well.

Summary of the Invention

It is an object of the present invention to provide a method for manufacturing semiconductor components with low contamination of metallic impurities in the active areas.

It is another object of the present invention to increase the yield and the reliability when manufacturing semiconductor components.

It is yet another object to minimize the leakage currents of semiconductor components.

It is still another object to achieve getter centres in semiconductor components without introducing dopants.

It is yet another object to achieve getter centres in semiconductor components without limiting the design options.

These objects are achieved according to the invention, by a semiconductor component having a device layer comprising at least one lateral insulating area, such as a trench, the walls of said lateral insulating area being covered with a gettering layer functioning as a getter when processing the semiconductor component.

Preferably, the gettering layer is substantially without acceptor and/or donor type impurities, or the concentration of acceptor and/or donor type impurities is not greater than the concentration of acceptor and/or donor type impurities in the trench wall.

The gettering layer comprises a gettering material such as polysilicon or porous silicon, or a silicide, and is covered with a layer of an insulating material, which may be, for example, silicon dioxide, a nitride, CVD oxide, TEOS, spin-on glass, or even teflon.

A method for the manufacturing of such a component is also disclosed, comprising the steps of

- masking and etching a trench extending through the upper silicon layer to a buried layer in the way common in the art,
- covering the walls of the trench with a layer of a gettering material.

Preferably, the following steps are also carried out:

- growing or depositing an oxide layer on the gettering layer in the trench.

- filling the trench with an insulating material or with polysilicon

The walls and/or bottom of the trench may be covered with a material that will function as a getter centre. This should be a material having high tension or a high density of grain boundaries, such as polycrystalline silicon or porous silicon. A silicide can also be used. Preferably, the trench is filled with polycrystalline silicon.

Although the component and the process have been discussed in this document for semiconductor components comprising at least one trench, the teachings of the invention may be applied to any semiconductor component in which lateral isolation is used, such as MESA (in which the silicon surrounding the active component is etched back so that the active component forms an elevated area on the silicon wafer) or STI (shallow trench isolation). Therefore, the word trench should be interpreted in the broadest sense, as meaning any form of lateral insulating region between components.

The invention offers the following advantages:
Getter zones may be introduced in the semiconductor without additional masking steps.
Lateral getter zones on SOI substrate enables the use of the whole silicon film in the vertical dimension for the active components without affecting the leakage current or the electric field pattern.
The flexibility regarding component design near the getter zone remains high compared to components using a doped region as a getter.

The getter centre is located closer to the active component than if located at the back of the component, (typically 10μm as opposed to at least 400μm) thus increasing the gettering effect.

Applying polysilicon to a doped trench wall will improve its function as a getter centre.

Brief Description of the Drawings

Figures 1A, 1B and 1C show prior art solutions to the problem of gettering impurities.

Figure 2 shows a semiconductor component according to the invention, using a trench wall to capture impurities.

Figure 3A-3D is a flow chart of the production process for an SOI component according to the invention.

Detailed Description of Embodiments

Figure 1A shows a prior art semiconductor component comprising several layers. The bottom layer 1 is a silicon substrate on which a silicon dioxide layer 3 has been formed or deposited. On top of the silicon dioxide layer 3, there is a silicon layer 5. The lower part 5a of the silicon layer 5 has been heavily doped, to function as a getter, that is, to attract the impurities. The upper part 5b of the silicon layer 5 is the layer comprising the active components.

The lower layer 5a of the silicon layer 5 in Figure 1A, may instead be a polysilicon layer, which will function as a getter.

Figure 1B shows another prior art semiconductor component. As in Figure 1A, there is a silicon substrate layer 11 with a buried silicon dioxide layer 13 on top. On top of the silicon dioxide layer 13, there is a silicon layer 15 comprising the active components. The silicon layer 15 comprises one or more heavily doped regions 15a, for lateral gettering of impurities. The remaining area 15b of the silicon layer 15 is the area comprising the active components.

Figure 1C shows a prior art semiconductor component . As in the previous figures, the component comprises a silicon substrate layer 21 with a buried silicon dioxide layer 23 on top. On the buried layer 23 there is a silicon layer 25. Parts 25b of the silicon layer 25 comprise the active components. A trench 27 has been formed to provide lateral isolation between the active components. The wall 29 of the trench 27 has then been doped and an oxide layer 31 has been grown or deposited on the trench wall outside the doped wall 29. The doped wall 29 functions as a getter centre. The trench 27 has also been filled, with polysilicon or an insulating material, in a way known in the art.

Figure 2 shows a semiconductor component in which metallic impurities are gettered according to the invention. An SOI component is used to describe the invention but, as will be readily understood by the skilled person, any semiconductor may be used. As in the previous figures, the component comprises a silicon substrate 101 with a buried layer 103 of silicon dioxide on top. On the buried layer, a silicon layer 105 comprising the active components is located. In the silicon layer 105 a trench 107 has been formed in a way common in the art, by masking and etching.

The walls 108 of the trench 107 have then been covered with a layer 109 of a material that will function as a getter, that is a material having high tension or a lot of grain boundaries, for example, polycrystalline silicon or porous silicon. The layer 109 has then been partly oxidized to form a layer 111 of silicon dioxide. Alternatively, the oxide layer 111 has been deposited. The trench 107 has also been filled, with polysilicon or an insulating material, in a way known in the art.

Figures 3A to 3D show important steps of the manufacturing process relevant to the production of getter centres according to the invention, that is, to produce the component shown in Figure 2:

Figure 3A shows a semiconductor component comprising a substrate layer 101', an insulating layer 103' and a silicon layer 105' in which a trench 107' has been formed using conventional masking and etching techniques. The region where the substrate faces the trench is referred to as the trench wall 108'. Before this stage, the surface of the component is covered with another oxide and/or nitride layer (not shown).

Figure 3B shows the same semiconductor component with a layer 109' of a gettering material deposited over the surface of the component, including the walls 108' and bottom of the trench. The layer 109' may be, for example, polysilicon or porous silicon, or a silicide.

Figure 3C shows the same semiconductor component after the layer 109' has been etched back from the top of the component and from the bottom of the trench, leaving a layer 109" of a gettering material, covering the trench walls 108'. The layer 109' does not have to be removed from the bottom of the trench, but usually is, for practical reasons, as conventional etching techniques will etch back a layer uniformly over its whole surface. The thickness of the remaining layer 109" covering the trench walls (108') is preferably between 500Å and 1μm.

Figure 3D shows the same semiconductor component after a layer of oxide 111' has been grown or deposited over the whole surface of the component. The trench 107' of the component shown in Figure 3D may then be filled with polysilicon, or an insulator such as silicon dioxide, a nitride, CVD oxide, TEOS, spin-on glass or teflon, to produce a component similar to the one shown in Figure 2.

The oxide layer 111' may be kept covering the component, or may be etched back before the subsequent steps.

As mentioned before, this procedure may be carried out at any point in the manufacturing process of the semiconductor. In order for the trench to function as a getter centre, however, it is desirable to create the trench according to the invention at an early stage, prior to the formation of any component parts sensitive to metallic impurities, such as the formation of the gate oxide or implantation of emitter regions. Even if made at a later stage, the trench according to the invention may still serve to reduce leakage currents but will not be able to getter impurities to the same degree as if it is present while the sensitive parts of the active components are being formed.

As mentioned above, the teaching of the invention are not limited to components comprising trenches, but may also be applied to MESA or shallow trenches. In these cases, the last step, in which the trench is filled with a suitable material, is not usually applicable.

Claims

1. A semiconductor component having a device layer (105; 105') comprising at least one lateral insulating area, such as a trench (107; 107'), **characterized** in that the walls (108; 108') of said lateral insulating area (107; 107') are covered with a layer (109; 109") functioning as a getter when processing the semiconductor component.

2. A semiconductor component according to claim 1, **characterized** in that the layer (109, 109") is substantially without acceptor and/or donor type impurities.

3. A semiconductor component according to claim 1, **characterized** in that the concentration of acceptor and/or donor type impurities in the layer (109; 109") is not greater than the concentration of acceptor and/or donor type impurities in the trench wall (108; 108').

4. A semiconductor component according to any one of the preceding claims, **characterized** in that the layer (109; 109") is covered with a layer (111) of silicon dioxide.

5. A semiconductor component according to any one of the preceding claims, **characterized** in that the layer (109; 109") comprises polysilicon or porous silicon.

6. A semiconductor component according to any one of the claims 1-4, characterized in that the layer (109; 109") comprises a silicide.

7. A semiconductor component according to any one of the preceding claims, characterized in that the layer (109; 109") comprises at least 50% silicon.

8. A semiconductor component according to any one of the preceding claims, characterized in that the thickness of the gettering layer is between 500Å and 1μm.

9. A semiconductor component according to any one of the preceding claims, **characterized** in that the trench (107) is filled with polysilicon or an insulating material.

10. A semiconductor component according to any one of the preceding claims, **characterized** in that the substrate layer (101) comprises silicon.

11. A semiconductor component according to any one of the preceding claims, **characterized** in that the buried layer (103) comprises silicon dioxide.

12. A semiconductor component according to any one of the preceding claims, **characterized** in that it is a silicon on insulator (SOI) component.

13. A method of producing a getter centre in a semiconductor component, said semiconductor component comprising a substrate layer (101; 101'), an upper silicon layer (105;105') and a buried layer (103; 103) isolating the substrate layer (101; 101') from the upper silicon layer (105; 105'),
said method comprising the steps of
- masking and etching a trench (107; 107') extending through the upper silicon layer (105; 105') to the buried layer (103; 103') in the way common in the art,
- covering the walls (108; 108')of the trench (107; 107') with a layer (109; 109")) of a gettering material.

14. A method according to claim 13, **characterized** by the step of
- growing or depositing an oxide layer (111; 111') on the gettering layer (109; 109") in the trench (107; 107').

15. A method according to claim 13 or 14, **characterized** by the step of
- filling the trench (107; 107')with an insulating material.

16. A method according to claim 13 or 14, **characterized** by the step of
- filling the trench (107; 107') with polysilicon, or with an insulating material.

17. A method according to any one of the claims 13-16, **characterized** by using polysilicon or porous silicon in the gettering layer (109; 109").

18. A method according to any one of the claims 13-16, **characterized** by using a silicide in the gettering layer (109; 109").

19. A method according to any one of the claims 13-18, **characterized** by using a material comprising at least 50% silicon in the gettering layer (109; 109").

20. A method according to any one of the claims 13-19, characterized by making the gettering layer (109; 109") between 500Å and 1μm thick.

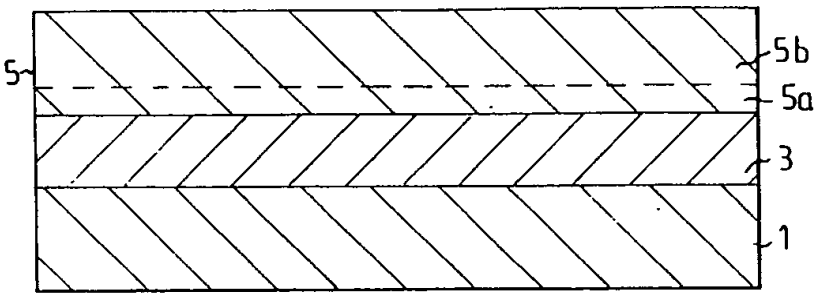

FIG. 1A

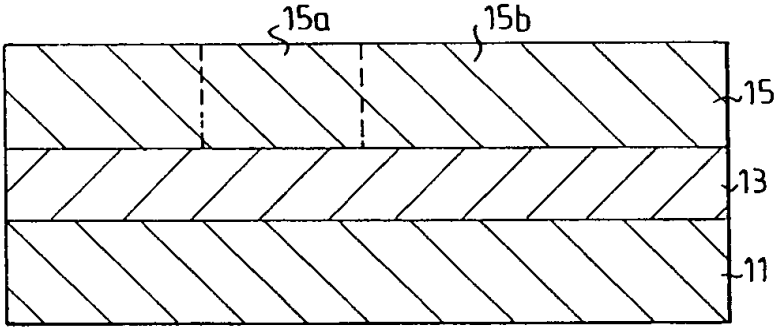

FIG. 1B

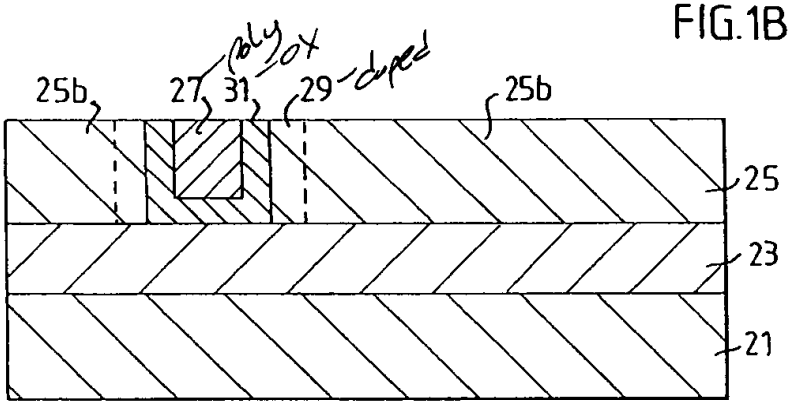

FIG. 1C

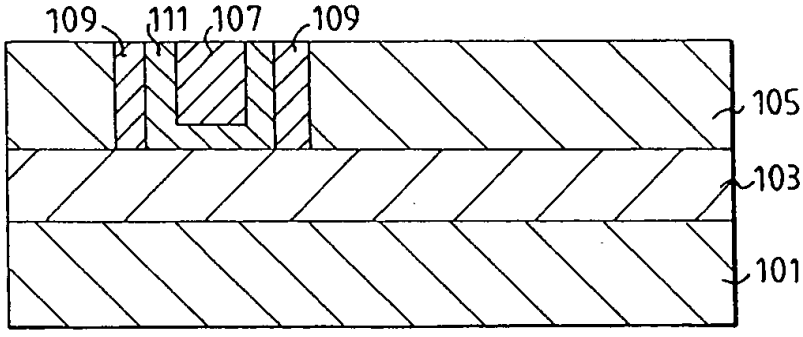

FIG. 2

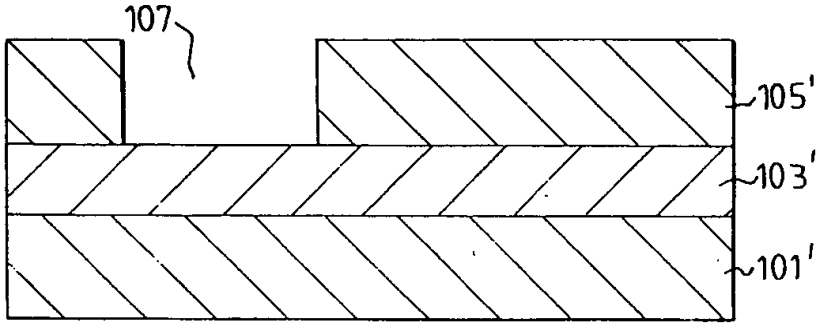

FIG. 3A

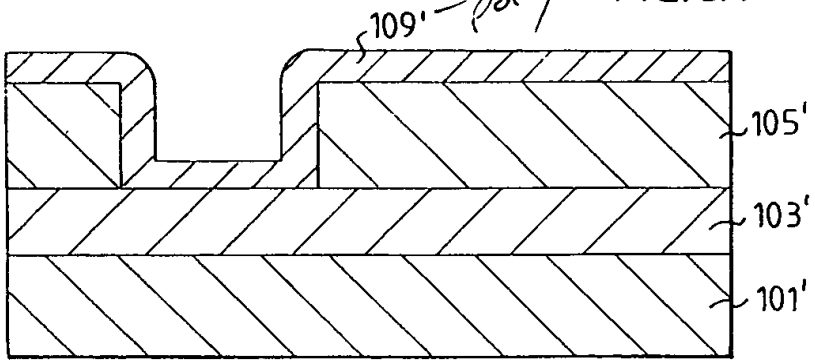

FIG. 3B

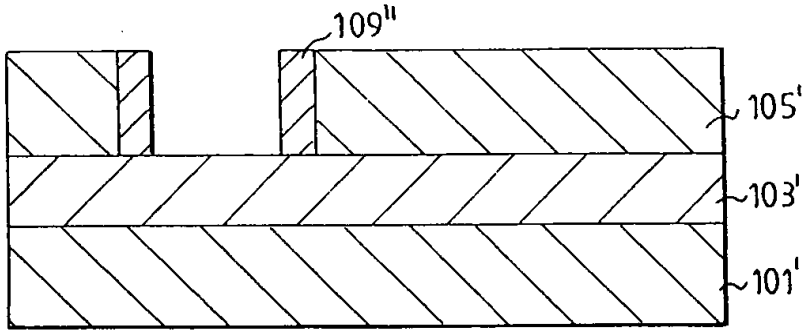

FIG. 3C

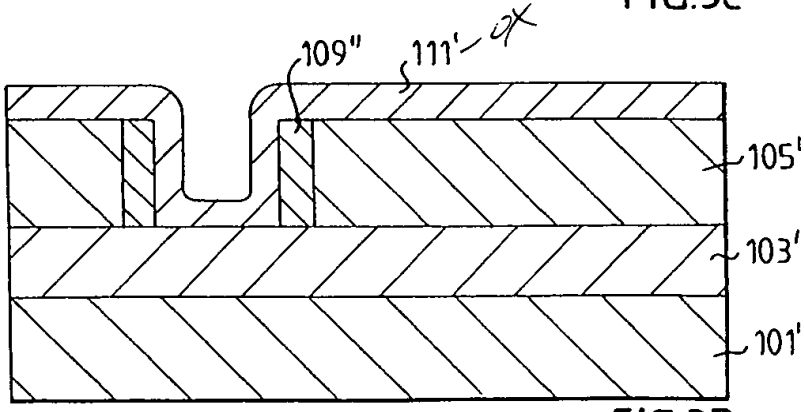

FIG. 3D